CLAIMS

What is claimed is:

1.   A controller, comprising:

a primary processing unit;

5   a secondary processing unit coupled to the primary processing unit;

a common memory coupled to the primary and secondary processing

units, the common memory containing a control algorithm, wherein the primary

and secondary processing units are adapted to run the control algorithm; and,

a functional compare module coupled to the primary processing unit and

10   the secondary processing unit for comparing a primary output of the primary

processing unit and a secondary output of the secondary processing units after

the control algorithm has been run by the primary and secondary processing

units.

15   2.   A controller, as set forth in claim 1, wherein the functional

compare module is adapted to detect a fault if the primary output and the

secondary output are not the same.

3.   A controller, as set forth in claim 1, wherein the primary output

20   and the secondary output are data.

4.   A controller, as set forth in claim 1, wherein the primary output

and the secondary output are control signals.

5.   A controller, as set forth in claim 1, wherein the functional compare module is adapted to perform diagnostics upon startup of the controller.

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6.   A controller, as set forth in claim 1, including at least one peripheral module coupled to the primary processing unit, wherein the at least one peripheral nodule includes a built in self test circuit for detecting faults within the peripheral module, the built in self test circuit being coupled to the

10   primary processing unit.

7.   A controller, as set forth in claim 1, including at least one bus, wherein the common memory, primary and secondary processing units, and functional compare module are coupled to the at least one bus, wherein the

15   functional compare module is adapted to read signals on the at least one bus, generate a signature of the signals, compare the generated signature with a reference signal and detect a fault if the signals are not the same.

8.   A controller, as set forth in claim 7, wherein the at least one bus

20   includes an address bus, a data bus, and a control bus.

9.   A controller, as set forth in claim 1, wherein the primary

processing unit is coupled to a system for control of the system, and wherein the

secondary processing unit is adapted to control the system if a fault is detected

in the primary processing unit.

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10.   A controller, as set forth in claim 9, wherein the secondary

processing unit is coupled to a second system for control of the second system.

11.   A method for detecting a fault in a controller, the controller

10   including a primary processing unit, a secondary processing unit coupled to the

primary processing unit, and a common memory coupled to the secondary and

primary processing units, including the steps of:

reading a control algorithm stored in the common memory by the

primary processing unit;

15   reading the control algorithm stored in the common memory by the

secondary processing unit;

comparing a primary output of the primary processing unit and a

secondary output of the secondary processing unit and responsively detecting a

fault.

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12.   A method, as set forth in claim 11, wherein the primary output

and the secondary output are data.

13.   A method, as set forth in claim 11, wherein the primary output and the secondary output are control signals.

14.   A method, as set forth in claim 11, including the step of

5   performing diagnostics upon startup of the controller.

15.   A method, as set forth in claim 11, wherein the controller includes at least one peripheral module coupled to the primary processing unit, the method including the step of detecting faults within the peripheral module

10   using a built in self test circuit coupled to the primary processing unit.

16.   A method, as set forth in claim 11, wherein the controller includes at least one bus, wherein the common memory, primary and secondary processing units, and functional compare module are coupled to the at least one

15   bus, and including the steps of:

reading signals on the at least one bus;

generating a signature of the signals;

comparing the generated signature with a reference signal; and,

detecting a fault if the signals are not the same.

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17.   A method, as set forth in claim 16, wherein the at least one bus includes an address bus, a data bus, and a control bus.

18.   A method, as set forth in claim 11, wherein the primary

processing unit is coupled to a system for control of the system, the method

including the step of controlling the system by the secondary processing unit if

a fault is detected in the primary processing unit.

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19.   A method, as set forth in claim 18, wherein the secondary

processing unit is coupled to a second system for control of the second system.

20.   An apparatus for controlling a first system of a motor vehicle,

10   comprising:

a primary processing unit for performing a first set of functions with

respect to the first system;

a secondary processing unit coupled to the primary processing unit;

a common memory coupled to the primary and secondary processing

15   units, the common memory containing a control algorithm, wherein the primary

and secondary processing units are adapted to run the control algorithm; and,

a functional compare module coupled to the primary processing unit and

the secondary processing unit for comparing a primary output of the primary

processing unit and a secondary output of the secondary processing units after

20   the control algorithm has been run by the primary and secondary processing

units.

21.   An apparatus, as set forth in claim 20, wherein the first system is a brake system.

22.   An apparatus, as set forth in claim 20, wherein the first system is a steering system.

23.   An apparatus, as set forth in claim 22, wherein the steering system is a steer by wire system.

24.   An apparatus, as set forth in claim 20, wherein the first system is an engine control system.

25.   An apparatus, as set forth in claim 20, wherein the functional compare module is adapted to detect a fault if the primary output and the secondary output are not the same.

26.   An apparatus, as set forth in claim 20, wherein the primary output and the secondary output are data.

27.   An apparatus, as set forth in claim 20, wherein the primary output and the secondary output are control signals.

28.   An apparatus, as set forth in claim 20, wherein the functional

compare module is adapted to perform diagnostics upon startup of the

apparatus.

5   29.   An apparatus, as set forth in claim 20, including at least one

peripheral module coupled to the primary processing unit, wherein the at least

one peripheral nodule includes a built in self test circuit for detecting faults

within the peripheral module, the built in self test circuit being coupled to the

primary processing unit.

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30.   An apparatus, as set forth in claim 20, including at least one bus,

wherein the common memory, primary and secondary processing units, and

functional compare module are coupled to the at least one bus, wherein the

functional compare module is adapted to read signals on the at least one bus,

15   generate a signature of the signals, compare the generated signature with a

reference signal and detect a fault if the signals are not the same.

31.   An apparatus, as set forth in claim 30, wherein the at least one

bus includes an address bus, a data bus, and a control bus.

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32.   An apparatus, as set forth in claim 20, wherein the secondary

processing unit is adapted to control the first system if a fault is detected in the

primary processing unit.

33.   An apparatus, as set forth in claim 32, wherein the secondary

processing unit is coupled to a second system for control of the second system.

5   34.   A method for detecting a fault in a controller for use in a motor

vehicle, the controller including a primary processing unit, a secondary

processing unit coupled to the primary processing unit, and a common memory

coupled to the secondary and primary processing units, including the steps of:

reading a control algorithm stored in the common memory by the

10   primary processing unit;

reading the control algorithm stored in the common memory source by

the secondary processing unit;

comparing a primary output of the primary processing unit and a

secondary output of the secondary processing unit and responsively detecting a

15   fault.

35.   A method, as set forth in claim 34, wherein the first system is a

brake system.

20   36.   A method, as set forth in claim 34, wherein the first system is a

steering system.

37.   A method, as set forth in claim 35, wherein the steering system is a steer by wire system.

36.   A method, as set forth in claim 34, wherein the first system is an

5   engine control system.

37.   A method, as set forth in claim 34, wherein the primary output and the secondary output are data.

10   38.   A method, as set forth in claim 34, wherein the primary output and the secondary output are control signals.

39.   A method, as set forth in claim 34, including the step of performing diagnostics upon startup of the controller.

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40.   A method, as set forth in claim 34, wherein the controller includes at least one peripheral module coupled to the primary processing unit, the method including the step of detecting faults within the peripheral module using a built in self test circuit coupled to the primary processing unit.

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41.   A method, as set forth in claim 34, wherein the controller

includes at least one bus, wherein the common memory, primary and secondary

processing units, and functional compare module are coupled to the at least one

bus, and including the steps of:

5   reading signals on the at least one bus;

generating a signature of the signals;

comparing the generated signature with a reference signal; and,

detecting a fault if the signals are not the same.

10   42.   A method, as set forth in claim 41, wherein the at least one bus

includes an address bus, a data bus, and a control bus.

43.   A method, as set forth in claim 34, wherein the primary

processing unit is coupled to a system for control of the system, the method

15   including the step of controlling the system by the secondary processing unit if

a fault is detected in the primary processing unit.

44.   A method, as set forth in claim 43, wherein the secondary

processing unit is coupled to a second system for control of the second system.

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45.   A controller for a motor vehicle, comprising:

a primary processing unit coupled to the motor vehicle and adapted to

perform a first set of functions;

a secondary processing unit coupled to the motor vehicle and to the

primary processing unit and adapted to perform a set of primary test functions;

a common memory coupled to the primary and secondary processing

units, the common memory containing a control algorithm, wherein the primary

5   processing unit is adapted to run the control algorithm; and,

a functional compare module coupled to the primary processing unit and

the secondary processing unit for comparing a primary output of the primary

processing unit after the control algorithm has been run and a test output of the

secondary processing units and to responsively detect a fault in the primary

10   processing unit, wherein the secondary processing unit is adapted to perform the

first set of functions upon detection of a fault in the primary processing unit.

46.   A controller, as set forth in claim 45, wherein the first system is a

brake system.

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47.   A controller, as set forth in claim 45, wherein the first system is a

steering system.

48.   A controller, as set forth in claim 46, wherein the steering system

20   is a steer by wire system.

49.   A controller, as set forth in claim 45, wherein the first system is

an engine control system.

50. A controller, as set forth in claim 45, wherein the secondary processing unit is adapted to perform a second set of functions, and wherein the primary processing unit is adapted to perform a set of secondary test functions, and wherein the functional compare module is adapted to detect a fault in the secondary processing unit, wherein the primary processing unit is adapted to perform the second set of functions upon detection of a fault in the secondary processing unit.

51. A method for detecting a fault in a controller for use in a motor vehicle, the controller including a primary processing unit coupled to the motor vehicle and adapted to perform a first set of functions and a common memory coupled to the primary and secondary processing units, the common memory containing a control algorithm, wherein the primary processing unit is adapted to run the control algorithm, wherein the method includes the steps of:

performing a set of primary test functions by the secondary processing unit;

comparing a primary output of the primary processing unit after the control algorithm has been run and a test output of the secondary processing units;

responsively detecting a fault in the primary processing unit; and,

performing the first set of functions by the secondary processing unit upon detection of a fault in the primary processing unit.

52.   A method, as set forth in claim 51, wherein the first system is a

brake system.

5   53.   A method, as set forth in claim 51, wherein the first system is a

steering system.

54.   A system, as set forth in claim 53, wherein the steering system is

a steer by wire system.

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55.   A system, as set forth in claim 51, wherein the first system is an

engine control system.

56.   A system, as set forth in claim 51, including the steps of:

15   performing a second set of functions by the secondary processing unit;

performing a set of secondary test functions by the primary processing

unit; and,

wherein the secondary processing unit is adapted to perform a set of

secondary test functions, and responsively detecting a fault in the secondary

20   processing unit; and,

performing the second set of functions by the primary processing unit

upon detection of a fault in the secondary processing unit.

57.   A controller for controlling a system, comprising:

a processing unit;

a common memory coupled to the primary processing unit, the common memory containing a control algorithm, wherein the primary processing unit is

5   adapted to run the control algorithm and to store data on the common memory during runtime of the control algorithm, wherein the controller is adapted to store a set of data values on the memory and a first signature of the data values determined in real-time and to subsequently retrieve the data, determine a second signature of the data values, compare the first and second signatures,

10   and to detect a fault of the common memory in response to the first and second signatures being different.

58.   A method for detecting a fault within a controller, the controller being adapted to control a system, and including a processing unit and a

15   common memory coupled to the primary processing unit, the common memory containing a control algorithm, wherein the primary processing unit is adapted to run the control algorithm and to store data on the common memory during runtime of the control algorithm, wherein the method includes the steps of:

storing a set of data values on the memory;

20   determining a first signature of the data values in real-time and storing the first signature on the common memory; and,

subsequently retrieving the data and determining a second signature of the data values; and,

comparing the first and second signatures and detecting a fault of the

common memory in response to the first and second signatures being different.